CLAIMS

What is claimed is:

1. An apparatus comprising:

an amplifier;

a first inverter having an input coupled to an output of the amplifier; and

a second inverter having an input coupled to an output of the first inverter and an output, wherein the output of the second inverter is fed back to an input of the amplifier.

2. The apparatus as claimed in claim 1, wherein the amplifier is a CMOS amplifier.

3. The apparatus as claimed in claim 2, wherein the CMOS amplifier is a hybrid Bazes and Chappell amplifier.

4. The apparatus as claimed in claim 3, wherein:

the amplifier includes a first, a second and a third pMOS transistor and a first, a second and a third nMOS transistor;

a gate of the first pMOS transistor and a gate of the first nMOS transistor are coupled to an input;

a gate of the second pMOS transistor and a gate of the first nMOS transistor are coupled to a drain of the first pMOS transistor and a drain of the first nMOS transistor; and

a gate of the third pMOS transistor and a gate of the third nMOS transistor are coupled to an inverse input.

5. The apparatus as claimed in claim 4, wherein the gate of the second pMOS transistor and the gate of the first nMOS transistor are coupled to the drain of the first pMOS transistor and the drain of the first nMOS transistor via a resistor.

6. The apparatus as claimed in claim 1, wherein the second inverter is approximately four times the size of the first inverter.

7. The apparatus as claimed in claim 1, wherein the first inverter is approximately one-fourth the size of the output of the amplifier.

8. The apparatus as claimed in claim 1, wherein the first inverter is approximately one-fourth the size of the output of the amplifier and the first inverter is approximately one-fourth the size of the second inverter.

9. The apparatus as claimed in claim 1, wherein the output of the second inverter is fed back to the amplifier as negative feedback.

10. The apparatus as claimed in claim 1, wherein the amplifier provides positive feedback.

11. The apparatus as claimed in claim 1, wherein the amplifier provides positive feedback and the output of the second inverter is fed back to the amplifier as negative feedback.

12. The apparatus as claimed in claim 11, wherein the amplifier mixes the positive feedback and the negative feedback.

13. The apparatus as claimed in claim 4, wherein the amplifier further includes a resistor, wherein the resistor is included in a circuit that mixes positive feedback provided by the amplifier and negative feedback provided to the amplifier from the output of the second inverter.

14. The apparatus as claimed in claim 1, further comprising an output, wherein the output is coupled to the output of the second inverter.

15. The apparatus as claimed in claim 1, wherein the output does not include precharge artifacts from the amplifier.

16. An apparatus comprising:

an amplifier; and

a delay and gain circuit coupled to an output of the amplifier, wherein an output of the delay and gain circuit is fed back to the amplifier.

17. The apparatus as claimed in claim 16, wherein the output of the delay and gain circuit is fed back to the amplifier as negative feedback.

18. The apparatus as claimed in claim 16, wherein the amplifier provides positive feedback.

19. The apparatus as claimed in claim 16, wherein the amplifier provides positive feedback and the output of the delay and gain circuit is fed back to the amplifier as negative feedback.

20. The apparatus as claimed in claim 19, wherein the amplifier mixes the positive feedback and the negative feedback.

21. The apparatus as claimed in claim 19, wherein the amplifier includes a resistor, wherein the resistor is included in a circuit that mixes the positive feedback and the negative feedback.

22. An amplifier comprising:

an input;

an inverse input;

an output;

a first pMOS transistor having a gate coupled to the input of the amplifier;

a second pMOS transistor;

a third pMOS transistor having a gate coupled to the inverse input of the amplifier and having a source coupled to a source of the first pMOS transistor and to a drain of the second pMOS transistor;

a first nMOS transistor having a gate coupled to the input of the amplifier;

a second nMOS transistor having a gate coupled to a drain of the first pMOS transistor, a drain of the first nMOS transistor, and to a gate of the second pMOS transistor; and

a third nMOS transistor having a gate coupled to the inverse input of the amplifier, a drain coupled to a drain of the third pMOS transistor and a source coupled to a source of the first nMOS transistor and to a drain of the second nMOS transistor, wherein the output of the amplifier is coupled to the drain of the third pMOS transistor and to the drain of the third nMOS transistor.

23. The amplifier according to claim 22, further comprising a resistor, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled directly together, and the drain of the first pMOS transistor and the drain of the first nMOS transistor are coupled directly together, wherein the direct coupling of the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled via the resistor to the direct coupling of the drain of the first pMOS transistor and the drain of the first nMOS transistor.

24. The amplifier according to claim 23, wherein the resistor has a resistance of approximately 5000 ohms.

25. The amplifier according to claim 22, further comprising a control input, wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled to the control input.

26. The amplifier according to claim 22, wherein a width of each of the first pMOS transistor, the second pMOS transistor and the third pMOS transistor is approximately 9.2um, and wherein a width of the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 4um.

27. The amplifier according to claim 26, wherein a length of each of the first pMOS transistor, the second pMOS transistor, the third pMOS transistor, the first nMOS transistor, the second nMOS transistor and the third nMOS transistor is approximately 80nm.

28. A system comprising:

a transmitter;

a receiver; and

a transmission line coupled to the transmitter and the receiver;

the receiver including:

an amplifier; and

a delay and gain circuit coupled to an output of the amplifier, wherein an output of the delay and gain circuit is fed back to the amplifier.

29. The system as claimed in claim 28, wherein the receiver is a high speed serial differential receiver.

30. The system as claimed in claim 28, wherein the delay and gain circuit comprises a first inverter and a second inverter.

31. The system as claimed in claim 30, wherein the first inverter is coupled to the output of the amplifier and the first inverter and the second inverter are connected in series.

32. The system as claimed in claim 31, wherein:

the amplifier includes a first, a second and a third pMOS transistor and a first, a second and a third nMOS transistor;

a gate of the first pMOS transistor and a gate of the first nMOS transistor are coupled to an input;

a gate of the second pMOS transistor and a gate of the first nMOS transistor are coupled to a drain of the first pMOS transistor and a drain of the first nMOS transistor; and

a gate of the third pMOS transistor and a gate of the third nMOS transistor are coupled to an inverse input.

33. The system as claimed in claim 32, wherein the gate of the second pMOS transistor and the gate of the first nMOS transistor are coupled to the drain of the first pMOS transistor and the drain of the first nMOS transistor via a resistor.

34. The system as claimed in claim 31, wherein the second inverter is approximately four times the size of the first inverter.

35. The system as claimed in claim 31, wherein the first inverter is approximately one-fourth the size of the output of the amplifier.

36. The system as claimed in claim 31, wherein the first inverter is approximately one-fourth the size of the output of the amplifier and the first inverter is approximately one-fourth the size of the second inverter.

37. The system as claimed in claim 28, wherein the output of the delay and gain circuit is fed back to the amplifier as negative feedback.

38. The system as claimed in claim 28, wherein the amplifier provides positive feedback.

39. The system as claimed in claim 28, wherein the amplifier provides positive feedback and the output of the delay and gain circuit is fed back to the amplifier as negative feedback.

40. The system as claimed in claim 39, wherein the amplifier mixes the positive feedback and the negative feedback.

41. The system as claimed in claim 39, wherein the amplifier includes a resistor that mixes the positive feedback and the negative feedback.

42. The system as claimed in claim 28, wherein a gain of the feedback is a same magnitude as a loss of the transmission line.

43. A method comprising:

providing delay and gain to an output of an amplifier; and

feeding back an output from the delay and gain to the amplifier.

44. The method as claimed in claim 43, further comprising applying positive feedback to the amplifier.

45. The method as claimed in claim 43, further comprising applying negative feedback to the amplifier.

46. The method as claimed in claim 43, further comprising applying positive feedback to the amplifier and negative feedback to the amplifier.

47. The method as claimed in claim 43, wherein at least one of the delay, gain and feedback counteract and compensate for a frequency dependent loss.

48. A method comprising:

amplifying an input signal; and

compensating for a frequency dependent loss by feeding back an output signal to the amplifying.

49. The method according to claim 48, wherein the compensating further includes adding at least one of a delay and a gain.

50. The method according to claim 48, wherein the feedback is a negative feedback and the negative feedback is delayed for a period of a smallest data bit.

51. A method comprising:

applying positive feedback to an amplifier; and

applying delayed negative feedback to the amplifier.

52. The method as claimed in claim 51, further comprising applying gain to the delayed negative feedback before it is fed back to the amplifier.

53. The method as claimed in claim 51, further comprising mixing the positive feedback and the negative feedback.

54. The method as claimed in claim 53, further comprising balancing a ratio of the mixed positive feedback and negative feedback to compensate for a frequency dependent loss.

55. The method as claimed in claim 53, the mixing further comprising providing a proportional amount of positive feedback and negative feedback to compensate for an inter-symbol interference.

56. The method as claimed in claim 51, wherein the positive feedback is applied immediately and the negative feedback is applied after some time.